WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a memory cell array; and

a photo-detector which is arranged in the memory cell array, the photo-detector including a photo-detecting semiconductor element constituting a static latch which holds a first state in its initial state, and which is changed into a second state from the first state when the photo-detecting semiconductor element is irradiated with light,

wherein photo-detection by said photodetector is used for stopping internal actions.

2. The semiconductor integrated circuit according to Claim 1, wherein said photo-detecting semiconductor element in a state of non-conduction is a MOS transistor constituting the static latch.

3. The semiconductor integrated circuit according to Claim 2, comprising a diode element as said photo-detecting semiconductor element,

wherein said diode element is connected in a reverse bias in parallel with said MOS transistor.

4. A semiconductor integrated circuit comprising:

photodetectors each including a semiconductor element and a photo-detecting semiconductor arranged in series on a current path and respectively placed in a state of conduction and in a

state of non-conduction when they are operable,

wherein a potential of a connection point between the semiconductor element in the state of conduction and the photo-detecting semiconductor element in the state of non-conduction varies according to the ratio between a current driving force varying when the photo-detecting semiconductor element in the state of non-conduction is irradiated with light and a current driving force of the semiconductor element in the state of conduction, and photo-detection by said photodetectors is used for stopping internal actions.

5. The semiconductor integrated circuit according to Claim 4, wherein said photo-detecting semiconductor element in the state of non-conduction is a MOS transistor.

6. The semiconductor integrated circuit according to Claim 4, wherein said photo-detecting semiconductor element in the state of non-conduction is a diode element connected in a reverse bias on said current path.

7. A semiconductor integrated circuit comprising:

a first circuit including a semiconductor element for sensitivity adjustment on a current path;

a second circuit whose photo-detection sensitivity is adjusted by said first circuit and which has a photo-detecting semiconductor element on a current path; and

a third circuit for detecting the output node level of the second circuit,

said semiconductor integrated circuit further comprising:

photodetectors for varying the output of said third circuit according to the output node level of said second circuit which is subject to current variations when said photo-detecting semiconductor element is irradiated with light,

wherein photo-detection by said photodetectors is used for stopping internal actions.

8. The semiconductor integrated circuit according to Claim 7, wherein said photo-detecting semiconductor element is a MOS transistor constituting said current path.

9. The semiconductor integrated circuit according to Claim 8,

wherein said photo-detecting semiconductor element is a diode element arranged in parallel with a part of the current path of said second circuit, and

wherein said diode element is connected in a reverse bias.

10. The semiconductor integrated circuit according to Claim 9, wherein a plurality of said diode elements are arranged in parallel.

11. The semiconductor integrated circuit according to Claim 10, wherein said plurality of diode elements to be ubiquitous on a semiconductor chip of the semiconductor integrated circuit.

12. The semiconductor integrated circuit according to Claim 1, wherein the memory cell array has a SRAM module in which static type memory cells are arranged in a matrix, and said photodetectors

are arranged in the memory cell array of said SRAM module in place of some of the static type memory cells replaced by the photodetectors.

13. The semiconductor integrated circuit according to Claim 12, further comprising a redundant configuration which compensates the lack of said static type memory cells.

14. The semiconductor integrated circuit according to Claim 12, further comprising an ECC circuit that can detect and correct data errors resulting from the absence of said static type memory cells replaced by the photodetectors.

15. The semiconductor integrated circuit according to Claim 1, wherein the memory cell array has a mask ROM in which unrewritable nonvolatile memory cells are arranged in a matrix, and said photodetectors are arranged in the memory cell array of said mask ROM in place of some of the nonvolatile memory cells.

16. The semiconductor integrated circuit according to Claim 1, wherein the memory cell array has a flash memory in which electrically rewritable nonvolatile memory cells are arranged in a matrix, and said photodetectors are arranged in the memory cell array of said flash memory in place of some of the nonvolatile memory cells.

17. The semiconductor integrated circuit according to Claim 4, further including a logic circuit module operated in synchronism with a clock signal,

wherein said photodetectors are arranged in said logic

circuit module.

18. The semiconductor integrated circuit according to Claim 7, further including a power supply circuit or a clock generating circuit,

wherein said photodetectors are arranged in said power supply circuit or clock generating circuit.

19. The semiconductor integrated circuit according to Claim 7, wherein the current driving force of said semiconductor element for sensitivity adjustment is adjustable.

20. The semiconductor integrated circuit according to Claim 1, wherein, the pn junctions in said photo-detecting semiconductor element, those placed in a reversely biased state are made greater in square measure than other junctions and higher in photo-sensitivity than other semiconductor elements of the same type.

21. The semiconductor integrated circuit according to Claim 1, further comprising a metal film or a polysilicon film for shading upper layers of semiconductor elements other than the photo-detecting semiconductor elements of said photodetectors.

22. The semiconductor integrated circuit according to Claim 1, wherein diodes connected in the reverse direction are connected to said photo-detecting semiconductor element in parallel.

23. The semiconductor integrated circuit according to Claim 4, further comprising a plurality of circuit modules, in each of which said photodetectors are arranged at random.

24. The semiconductor integrated circuit according to Claim

7, further comprising a plurality of circuit modules, in each of which said photodetectors are arranged regularly.

25. The semiconductor integrated circuit according to Claim 4, wherein includes basic cells each comprising a pair of a basic element of a logic circuit and said photodetector are used.

26. The semiconductor integrated circuit according to Claim 25, wherein a plurality of said basic cells are distributively arranged.

27. A semiconductor integrated circuit comprising:

a memory cell array;

a logic circuit module;

a plurality of first photodetectors which is arranged in the memory cell array, the plurality of first photodetectors each including a photo-detecting semiconductor element constituting a static latch which holds a first state in its initial state, and are changed into a second state from the first state, when the photo-detecting semiconductor element is irradiated with light, wherein photo-detection signals provided by the first photodetectors are used for stopping internal actions of the logic circuit module; and

a plurality of second photodetectors which is arranged in the logic circuit module, the plurality of second photodetectors each including a semiconductor element and a photo-detecting semiconductor element arranged in series on a current path and respectively placed in a state of conduction and in a state of

non-conduction when they are operable, wherein a potential of a connection point between the semiconductor element in the state of conduction and the photo-detecting semiconductor element in the state of non-conduction varies according to the ratio between a current driving force varying when the photo-detecting semiconductor element in the state of non-conduction is irradiated with light and the current driving force of the semiconductor element in the state of conduction, and wherein photo-detection by said second photodetectors is used for stopping internal actions.

28. The semiconductor integrated circuit according to Claim 27, comprising:

a first circuit having a semiconductor element for sensitivity adjustment on a current path;

a second circuit whose photo-detection sensitivity is adjusted by said first circuit and which has a photo-detecting semiconductor element on a current path; and

a third circuit for detecting the output node level of the second circuit,

said semiconductor integrated circuit further comprising in an analog circuit a plurality of third photodetectors for varying the output of said third circuit according to the output node level of said second circuit which is subject to current variations when said photo-detecting semiconductor element is irradiated with light,

wherein photo-detection by said third photodetectors is used for stopping internal actions.

29. The semiconductor integrated circuit according to Claim 1, further including a reset circuit capable of making the logical sum signal of the photo-detection signals provided by the individual photodetectors a reset signal for initializing the interior and stopping the operation.

30. An IC card on a card substrate, the IC card comprising:

an external interfacing section; and

a semiconductor integrated circuit, according to Claim 27, connected to said external interfacing section.

31. The semiconductor integrated circuit according to Claim 29, wherein active shield wiring is connected to the transmission path of the logical sum signal of said photo-detection signals.

32. The semiconductor integrated circuit according to Claim 1, further including:

a voltage detecting circuit for outputting a voltage detection signal which varies in response to an undesired fall of the operating voltage; and

a reset circuit capable of making the logical sum signal of said voltage detection signal and said photo-detection signals provided by the individual photodetectors a reset signal.

33. The semiconductor integrated circuit according to Claim 1, further including:

a frequency detecting circuit for outputting a frequency

detection signal which varies in response to an undesired variation of the clock signal frequency, and

a reset circuit capable of making the logical sum signal of said frequency detection signal and said photo-detection signals provided by the individual photodetectors a reset signal.

34. The semiconductor integrated circuit according to Claim 1, further including:

a wiring cutoff detecting circuit for outputting a wiring cutoff detection signal which varies in response to any cutoff of prescribed internal wiring; and

a reset circuit capable of making the logical sum signal of said wiring cutoff detection signal and said photo-detection signals provided by the individual photodetectors a reset signal.

35. A semiconductor integrated circuit comprising:

photodetectors each including a photo-detecting semiconductor element and a metal film or polysilicon film for shading the upper layers of semiconductor elements other than said photo-detecting semiconductor element,

wherein said photo-detecting semiconductor element holds a state of non-conduction in its initial state, and photo-detection by said photodetectors, achieved by reversing said photo-detecting semiconductor element in a state of non-conduction into a state of conduction, is used for stopping internal actions.

36. The semiconductor integrated circuit according to Claim

12, wherein a plurality of said photodetectors are distributively arranged.

37. A semiconductor integrated circuit comprising:

photodetectors each including a first circuit having a photo-detecting semiconductor element on a current path, and a second circuit for detecting the output node level said first circuit,

wherein the output node of said first circuit strides over the logical threshold of the second circuit in accordance with a current varying when said photo-detecting semiconductor element is irradiated with light, a metal film or polysilicon film for shading the upper layers of other semiconductor elements than said photo-detecting semiconductor element is provided, and

wherein photo-detection by said photodetectors is used for stopping internal actions.